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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,592	09/10/2003	Seung-Bin You	8028-35	5319

(SPX200208-0021US

EXAMINER

YOUNG, BRIAN K

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 04/06/2004

7590 04/06/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/659,592

Applicant(s)

YOU, SEUNG-BIN

Examiner

Brian Young

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4 and 11 is/are allowed.
- 6) ☒ Claim(s) 5, 12 and 13 is/are rejected.
- 7) ☒ Claim(s) 6-10 and 14-20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 September 2003 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

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1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by McCarroll et al.

Claim 5 recites “An analog-to-digital (“A/D”) converter comprising a converter portion having at least three pipelined stages for receiving an analog input and generating a digital output, and an error correction portion in signal communication with the second of the at least three stages for correcting an error caused in the first of the at least three stages by updating an error correction bit”.

McCarroll et al disclose (title) “Digital calibration for analog-to-digital converters with implicit gain proration”. McCarroll et al disclose (col.3, Ins.33-43) “FIG. 3 specifically shows a two-stage, pipelined, analog-to-digital converter with an overall resolution of n bits, a resolution of m bits in the first stage, and a resolution of $n-m+1$ bits in the presumed ideal second stage, **with one bit of error correction**. The first stage is assumed to have both gain and DAC non-linearity errors. **The second ideal stage measures these errors and generates correction coefficients which, in the normal conversion mode, are addressed depending on the state of the first stage, and are digitally added to correct for the first-stage errors. In practice, the ideal stage is comprised of one or more pipelined stages**”.

Thus McCarroll et al specifically show how error correction is achieved in a pipelined ADC converter system.

3. Claims 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lim et al.

Claim 12 recites "A method of converting an analog input signal into a digital output signal, the method comprising: receiving an analog input signal, and providing at least one subsequent stage of a multi-stage pipelined structure for converting a portion of the received analog signal into a plurality of digital bits without an error bit".

Claim 13 further recites the use of sample and hold circuitry and overlapping an LSB with a MSB.

Lim et al disclose a (title) "**Pipelined multi-stage analog-to-digital converter**". Lim et al specifically disclose (col.5 lns.7-63) "In FIG. 6, an analog signal is input via a **sample-and-hold (S/H) circuit 1** which repeatedly samples the analog input signal at a certain time interval and holds a constant output value (voltage) corresponding to the most recent sampling. Then, in the first stage S1 receiving the voltage value from the S/H circuit 1, a first flash ADC 5 determines a most significant bit (MSB) consisting of n.sub.1 bits. Meanwhile, a digital code of the n.sub.1 bits is changed back into an analog representation by DAC means (not shown) within a first MDAC 10 of the first stage S1, and a reconstructed analog signal is obtained therein. The pipelined four-stage ADC as shown in FIG. 6 also includes a digital correction logic circuit 40 coupled

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to receive partial conversion outputs from the first, second, third and fourth stages for digital correction; a digital calibration logic circuit 50 for calibrating digital codes of the front stage of the pipelined four-stage ADC; and a digital subtractor 60 for outputting a digital output signal. The combined resolution of the ADC shown in FIG. 6 is the sum of the number of bits for each stage in the four-stage architecture, ***minus one overlapping bit between each of the respective stages***, or $n_{\text{sub.1}} + n_{\text{sub.2}} + n_{\text{sub.3}} + n_{\text{sub.4}} - 3$ bits. Here, the ***three overlapping bits are used for bit correction*** when an error is generated due to the MDAC gain error, lowresolution flash ADC error, etc.

Lim et al also recite (col.8, lns.39-43) "Gain errors, however, can be generated between the respective pipelined stages. For example, if an error is generated by ***overlapping the LSB of a former stage and the MSB in the following stage***, a gain error correction operation is performed".

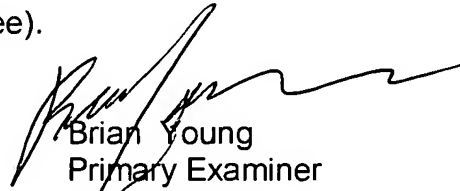
4. Claims 1-4 and 11 are allowed.

5. Claims 6-10 and 14-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Brian Young
Primary Examiner
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